REMARKS/ARGUMENTS

Claims 5-28 are pending and rejected.

Claims 5-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Keller (Patent No. 6,622,237) in view of Feiste (Patent No. 6,349,382). Claims 22-28 are rejected under 35 U.S.C. § 102(e) as being anticipated by Keller (Patent No. 6,622,237). Claims 10-12 and 18-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Keller and Feiste, and further in view of Abramson (Patent No. 5,898,854) and Hennessy (Computer Organization and Design).

Applicants respectfully submit the cited references fail to teach or suggest at least a scheduling method for a load microinstruction, comprising: if a new load microinstruction is admitted, predicting whether collision occurs between load microinstruction and an older store microinstruction, and if a collision is detected, determining whether data for the older store microinstruction is available in a store unit (*e.g.*, as described in claim 5).

Such a feature is not shown nor suggested in Keller. In Keller, the STLF predictor is trained with prior re-executions of load instructions. If the predictor provides an indication that a load instruction coming into the system has previously been identified in the STLF predictor, then that load instruction is scheduled after the corresponding store instruction identified in the STLF predictor (see Col. 12, lines 38-43). There is no disclosure nor suggestion in Keller to determine whether data for the store instruction is available.

As to the remaining independent claims, claims 22 and 27, these claims deal specifically with the STA and STD uop pair of a store instruction. The current Office Action cites to large sections of Columns 5 and 6 to show the features discussed in these claims. The cited sections,

however, only refer generally to the decoding of macroinstructions. The cited sections do not teach or disclose the specific features related to these claims.

To make up for the deficiencies of Keller, the Office Action asserts Feiste discloses the relevant limitations, citing practically the entire column 5 of the cited reference (lines 14-67). *See* Office Action dated 10/27/2008, page 3. Applicants disagree. To illustrate the cited reference fails to teach or suggest the relevant limitations, Applicants will discuss the section in summary.

Cited Figure 4 describes a flow diagram for store forwarding. In step 401, an effective address for a load instruction is computed. In step 402, the effective address is compared with an older store instruction in execute. If there is no overlap in step 403, the method proceeds to steps 404, 405, 406, and 407, which describe how the load instruction is serviced as normal. If there is an overlap (step 403), then the load instruction is rejected in step 404. In particular, if there is an overlap of the effective address between the store instruction in the store reorder queue 222 and the load instruction, then in step 408, a DATA VALID signal is disabled for the load instruction. In step 409, a determination is made of which is the youngest store instruction in the SRQ 222 that matches with the load instruction. In step 410, a determination is made whether this store instruction is forwardable. Steps 411 to 416 are directed to 1) formatting the read data and returning it to result busses and 2) determining what is done if the data is not resident in a store data queue.

Applicants submit the cited section fails to teach the relevant limitations. In particular, determining whether the youngest store instruction in a store reorder queue matches with a load instruction is not the same as predicting whether collision occurs between load microinstruction

and an older store microinstruction, and if a collision is detected, determining whether data for the older store microinstruction is available in a store unit (*e.g.*, as described in claim 5). Therefore, Applicants maintain the cited reference fails to teach or suggest the at least these relevant limitations, and the current rejection is lacking and should be withdrawn.

With regard to the §102 rejection of claims 22 and 27, Applicants maintain they do not teach or suggest at least the determining operation of claims 5 and 14 nor the STA/STD uop pair features of claims 22 and 27. First, Applicants note the Office Action has altered the rejection of claims 22-28 substantially, despite the fact that no amendments were made to the claims in the previous response. Applicants submit this is improper; the finality of the instant Office Action should be withdrawn and a new rejection should be issued in a non-final Office Action.

Regardless, the new rejection fails to address the relevant limitations as well. The Office Action asserts column 11, lines 25-31, column 12, lines 7-22, and column 12, lines 44-46 teach the relevant limitations. *See* Office Action dated 10/27/2008, page 8. Applicants disagree. Column 11, lines 25-31 describe a store ID field in a schedule buffer which may indicate, for example, a retry indication or a train indication (indicating a load is detected). Column 12, lines 7-22 are directed to detecting stores that interfere with load operations. Neither of these two sections address the relevant limitations; indeed, dependency pointers and the STA/STD uop pair features of claims 22 and 27 are not addressed at all. Finally, column 12, lines 44-47 are directed to describing inhibiting scheduling of a load until after a store instruction is schedule in the case where an interference occurs. Applicants submit this section fails to address the relevant limitations of claims 22 and 27, and that the entire Keller reference fails to teach or suggest the relevant limitations of claims 22 and 27.

Moreover, Abramson and Hennessy fail to make up for the deficiencies of Keller and Feiste. These references have been cited for specific features in the dependent claims. Abramson is directed to a buffer management scheme for load operations that permits load operation to be stored for execution to memory. Hennessy is a text directed to general principles of instruction processing. Neither of these two references address the relevant limitations of claims 5, 14, 22, and 27 discussed above.

Therefore, since for at least the above reasons, the cited references fail to teach or suggest at least the above-discussed limitations of claims 5, 14, 22, and 27, Applicants submit the rejections are lacking and should be withdrawn. Moreover, Applicants submit claims 5, 14, 22, and 27 are allowable, and claims 2-13, 15-21, 23-26, and 28-29 are allowable at least for depending from allowable base claims.

In view of the above, reconsideration and withdrawal of the rejection of claims 5-28 under 35 U.S.C. §§ 102(e) and 103(a) is respectfully requested.

The Office is authorized to charge any fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

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